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| **Reference Flows**  |
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| **SMIC-Synopsys Reference Flow 6.0** SMIC-Synopsys Reference Flow 6.0 delivers chip-level flat and hierarchical design flows from RTL to GDSII. The Reference Flow uses SMIC’s advanced 28-nanometer High-K Metal Gate (HKMG) process with the Synopsys Galaxy Design Platform, and all the scripts are compatible with the Synopsys Lynx Design System. Anchored by Synopsys' Design Compiler, IC Compiler/IC Compiler II, PrimeTime Suite, StarRC, IC Validator, DFTMAX, TetraMAX, VCS, Formality and PrimeRail, the Galaxy Design Platform reduces design cycle, decreases flow integration costs and helps minimize risks inherent in advanced, complex IC design. This proven reference flow was validated using the SMIC 28nm multi-VT and multi-channel standard cell libraries, Power Management Kit, Memory Macros, SMIC in-house PLL and IO to illustrate a multi-voltage design. In addition, the reference flow leverages IEEE-1801 Unified Power Format (UPF) to drive low power design physical implementation to improve the way complex System-on-Chip (SoC) designs are implemented and verified.SMIC and Synopsys’ collaboration enables IC designers to accelerate their designs into manufacturing, with a flexible, lower-risk design system and faster time-to-market with SMIC’s 28nm process technology.**SMIC-Synopsys Reference Flow 6.0 Benefits:** * SMIC 28nm technology RTL2GDSII physical design flow
* Advanced SMIC 28nm design rule support
* Full chip UPF low power design
* UPF low power verification
* Multi-VT & multi-channel libraries for leakage reduction optimization
* IC Validator based In-Design physical verification & chip finishing
* Efficient Automatic DRC Repair (ADR)
* DFM VIA insertion and Dummy Fill
* Advanced timing and SI signoff
* Test synthesis and power-aware ATPG
* All scripts are compatible with the Synopsys Lynx Design System

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**SMIC-Synopsys Reference Flow 6.0** **The SMIC-Synopsys Reference Flow 6.0 package includes:** * Design flow scripts
* Technology and library preparation scripts
* Comprehensive block level and chip level designs for flat implementation and hierarchical implementation.
* Flow setup and flow execution manual

For additional support, we have trained experts ready to support and offer you professional advice to bring your design to high-quality sign-off GDSII.If you would like to know more about the SMIC-Synopsys 28nm Reference Flow, please contact your SMIC account manager, login to [SMIC Now](http://service.smics.com/globallogin/index.action) or [send us a message](http://www.smics.com/eng/contact_us.php). |

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