# SMIC-Cadence Reference Flow 6.0

The SMIC-Cadence Reference Flow 6.0 is a digital reference flow which combines SMIC 28nm process technology and Cadence advanced RTL to GDSII low power digital solution. SMIC-Cadence RF6.0 incorporates Cadence design, implementation and signoff tools and solutions into a high automatic flow with a set of integrated flow scripts, and provides a set of frequently-used reference settings at SMIC 28nm in Cadence solution to designers, in order to save designer’s time in flow building and setting adjustment, and to help designers meet PPA (performance, power and area) target with less time. SMIC-Cadence RF6.0 help designers reduce turn-around time from front-end design, back-end implementation and signoff solutions, to meet the more and more strict design needs in computer, tablets, consumer electronics, and network markets.

SMIC-Cadence RF6.0 integrates SMIC/ARM IP and SMIC technology files:

* ARM standard cell library and low power design kit at SMIC 28nm HKMG process with Multi-Vt
* SMIC 28nm SRAM IP by ARM memory compiler
* SMIC 28nm HKMG GPIO and PLL IP
* SMIC 28nm HKMG Quantus QRC extraction technology files
* SMIC 28nm HKMG PVS DRC, LVS, and dummy insertion rule decks
* SMIC 28nm HKMG LPA pattern matching file and CCP model file, etc

SMIC-Cadence RF6.0 integrates and highlights Cadence advanced digital solutions:

* Chip-level design flow with SMIC 28nm process technology
* Cadence low power solution with IEEE1801-2013
* Genus and RC power and physical aware logical synthesis
* Conformal power aware logical equivalence check and low power extended validation
* Encounter Test ATPG
* Innovus and EDI flat and hierarchical implementation flows with GigaPlace and GigaOpt advanced engines
* Innovus and EDI multi-Vt swapping for power aware optimization
* Innovus with T-Quantus RC extraction which has best correlation to signoff
* Innovus in-design DRC signoff and metal fill
* Innovus in-design litho hotspot check and fixing
* Quantus multi-corner parallel RC extraction
* Tempus MMMC/DMMMC timing and SI signoff
* Voltus power and EMIR analysis, and powering-up analysis
* Voltus-Fi to Voltus hierarchical IR drop analysis solution
* PVS DRC/LVS signoff and model-based dummy insertion
* LPA litho hotspot check
* CCP thickness variation prediction

SMIC-Cadence RF6.0 package includes:

* Flow scripts, Tcl based, for running the whole flow with minimum manual intervene
* Flow configuration file, for library and technology file definition
* A demo design including RTL, SDC, and IEEE1801-2013 file for low power design flow demonstration
* A flow usage guideline document

